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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/540,220	01/09/2006	Paul Dischamp	0579-1096	5135

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EXAMINER	
BRITO PEGUERO, MERLIN	
ART UNIT	PAPER NUMBER
2887	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/540,220	DISCHAMP ET AL.	
	Examiner	Art Unit	
	Merlin Brito Peguero	2887	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *20 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/20/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file 06/20/05.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-10, 18, and 19 rejected under 35 U.S.C. 102(b) as being anticipated by Fallah (US 20020047781 A1.)

Re claim 1 and 2: Fallah discloses a secure electronic entity (ii) [1,30], characterized in that it contains means (18) for measuring time [13, 34] and in that it comprises means (21) for certifying an item of data relating to a date or a duration, said certification means (21) receiving [13, 34] from said time measuring means (18) information on said date and producing data certifying said item of data relative to a duration intended for an external entity (see figs: 1, 2, ¶'s: 0022 and 0025 central processing unit is capable of detecting time and certification of the time data is recorded.)

Re claim 3: Fallah discloses certification means (21) are adapted to certify the authenticity of a duration (see ¶: 0019, 0025, 0026, 0029, 0031 Fallah's card can

communicate date with external unit once the external unit provides an authentication code. The card therefore provides authenticated data)

Re claim 4: Fallah discloses certification means (21) are adapted to certify that an action has been effected in a given time period (see ¶: 0029 certifies temperature for a given time period.)

Re claim 5: Fallah discloses includes synchronization means (18a) (see ¶: 0019 the card can synchronize itself to the external unit.)

Re claim 6: Fallah discloses characterized in that said certification means (21) use authentication means (see ¶: 0026, 0031 authentication in the form of a password, cryptographic means allow access to data stored in memory of the card.)

Re claim 7 and 8: Fallah discloses time measuring means (18) are adapted to supply a measurement of time when said electronic entity (II) is not supplied with power by an external power supply and not supplied with electrical power (see 0027-0028 card is setup to take measurements at different time intervals, for example at every hour, that time stamp says when the system is powered to take data and when it is not powered to take data, i.e. before the hour not powered, for the time measurement powered.)

Re claim 9: Fallah discloses time measuring means (18) are adapted to supply a time measurement independently of any external clock signal (see ¶: 0029 the time is provided by the card.)

Re claim 10: Fallah discloses time measuring means (18) include means for comparing two dates (see ¶: 0019, 0025, 0029 data can be compared by means of the external unit.)

Re claims 18 and 19: Fallah discloses electronic entity that is portable, and a microcircuit card (see ¶: 005, 0025, and 0029.)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11-13 rejected under 35 U.S.C. 103(a) as being unpatentable over Fallah (US 20020047781 A1) in view of Horvat et al. (US 7036018 B2.)

Re claims 11-17: Fallah fails to teach a one subsystem (17) comprising a capacitive component (20) having a leak across its dielectric space, means for coupling said capacitive component to an electrical power supply for it to be charged by said electrical power supply, and means (22) for measuring the residual charge in the capacitive component (20), said residual charge being at least in part representative of the time that has elapsed since the capacitive component (20) was decoupled from the electrical power supply. Means (22) for measuring the residual charge are part of said time measuring means (18). Capacitive component (20) is a capacitor implemented in the MOS technology and whose dielectric space consists of silicon oxide. Means (22) for measuring the residual charge comprise a field- effect transistor (30) having an insulative layer (34), in that the capacitive component (20) includes an insulative layer (24), and in that the thickness of the insulative layer (34) of the field-effect transistor (30) is much greater than the thickness of the insulative layer (24 of the capacitive

component (20). The thickness of the insulative layer (24) of the capacitive component (20) is from 4 nanometers to 10 nanometers. Characterized in that it includes at least two subsystems (17A, 17B) each comprising a capacitive component having a leak across its dielectric space, means for coupling said capacitive component to an electrical power supply for it to be charged by said electrical power supply, and means for measuring the residual charge in the capacitive component, said residual charge being at least in part representative of the time that has elapsed since the capacitive component was decoupled from the electrical power supply, said subsystems (17A, 17B) comprising capacitive components having different leaks across their respective dielectric spaces, and in that said secure electronic entity (II) further includes means (14, 15, T) for processing measurements of the respective residual charges in said capacitive components to extract from said measurements information substantially independent of heat input to said entity (ii) during the elapsed time. Characterized in that said processing means (14, 15, T) include software for calculating a predetermined function for determining said information as a function of said measurements substantially independently of the heat input.

Horvat et al. teaches a one subsystem (17) comprising a capacitive component (20) having a leak across its dielectric space, means for coupling said capacitive component to an electrical power supply for it to be charged by said electrical power supply, and means (22) for measuring the residual charge in the capacitive component (20), said residual charge being at least in part representative of the time that has elapsed since the capacitive component (20) was decoupled from the electrical power

supply (see C: 6.) Means (22) for measuring the residual charge are part of said time measuring means (18) (see C: 6 L: 4-38). Capacitive component (20) is a capacitor implemented in the MOS technology and whose dielectric space consists of silicon oxide (see C: 6 L: 21-67.) Means (22) for measuring the residual charge comprise a field- effect transistor (30) having an insulative layer (34), in that the capacitive component (20) includes an insulative layer (24), and in that the thickness of the insulative layer (34) of the field-effect transistor (30) is much greater than the thickness of the insulative layer (24 of the capacitive component (20) (see C: 6 L: 39-67, and C: 7 L: 1-40.) The thickness of the insulative layer (24) of the capacitive component (20) is from 4 nanometers to 10 nanometers (see C: 6 L: 39-67 it is a matter of design choice as to the thickness of the insulating layer depending on how much charge will be stored.) Characterized in that it includes at least two subsystems (17A, 17B) each comprising a capacitive component having a leak across its dielectric space, means for coupling said capacitive component to an electrical power supply for it to be charged by said electrical power supply, and means for measuring the residual charge in the capacitive component, said residual charge being at least in part representative of the time that has elapsed since the capacitive component was decoupled from the electrical power supply, said subsystems (17A, 17B) comprising capacitive components having different leaks across their respective dielectric spaces, and in that said secure electronic entity (II) further includes means (14, 15, T) for processing measurements of the respective residual charges in said capacitive components to extract from said measurements information substantially independent of heat input to said entity (ii)

during the elapsed time (see C: 6 L 39-67 and C:7 L: 1-40.) Characterized in that said processing means (14, 15, T) include software for calculating a predetermined function for determining said information as a function of said measurements substantially independently of the heat input (see C: 6 the system has software that is controlled by the processor which is needed to operate the card.)

It would have been obvious, at the time of invention, to have combined Fallah electronic label with Horvat et al. integrated security card with the motivation that this would provide for a more reliable label by allow the card to carry a charge after being disconnected. Furthermore, it would provide for a greater security since the card allows for detection of tampering if for example disconnected from power supply.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nara et al. (US 4766294) which discloses an IC card.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Merlin Brito Peguero whose telephone number is (571) 270-1619. The examiner can normally be reached on Monday-Fridays 7:30 to 5:00 alt Fridays ET time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve S. Paik can be reached on (571) 272-2404. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Merlin Brito Peguero
Patent Examiner
01/16/2008

STEVEN S. PAIK
PRIMARY EXAMINER